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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 10

Application Number: 09/208,325
Filing Date: December 09, 1998
Appellant(s): SHIELDS ET AL.

H. Donald Nelson
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 3/4/01.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

A correct statement of the status of the claims is as follows:

Claim 1 is rejected under 35 U.S.C§ 102(e) as being anticipated.

Claims 1, 3-4 are rejected under 35 U.S.C§ 103(a).

In view of the appeal brief, claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct. However, this matter is petitionable not appealable.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant states issues in the brief. The issues should be as follow.

1- Claim 1 is rejected under 35 U.S.C. 102 (e) as being anticipated by Xing et al.

2- Claims 1 and 3-4 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Xing et al. in view of the Admitted Prior Art.

3- The proposed amendment after final was not enter. This issue relates to petitionable subject matter under 37 CFR 1.181 and not to appealable subject matter. See MPEP §§ 1002 and 1201.

(7) Grouping of Claims

Appellant states that each of the rejected claims stands on its own recitation, the claims being considered to be separately patentable.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,880,026	Xing et al.	3-1999

The Admitted Prior Art, Figures 1A-1I, pp. 1-2 of the specification.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Xing et al. (U.S. Patent No. 5,880,026).

Referring to figures 1-3D, Xing et al teaches a method of manufacturing a semiconductor device, wherein the method comprises: forming a final layer (see col. 5, lines 50-54) of metal (210, 230, 240, 250,) on a layer of interlayer dielectric (270) in the semiconductor device; forming a layer of TiN (205) on the final layer of metal; forming a first layer of photoresist (200) on the layer of TiN; patterning and developing the first layer of photoresist exposing portions of the layer of TiN (see figure 2A and related text); etching holes in the layer of TiN and the final layer of metal exposing portion of interlayer dielectric (see figure 2B), wherein metal structures are formed; removing the first layer of photoresist (see figure 2B and related text); removing the remaining portions of the layer of TiN (see figure 2C); and forming a blanket layer of interlayer dielectric on the surface of the semiconductor device (280).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xing et al. (U.S. Patent No. 5,880,026) in view of the Admitted Prior Art (pp. 1-2).

Referring to figures 1-3D, Xing et al teaches a method of manufacturing a semiconductor device, wherein the method comprises: forming a final layer (see col. 5, lines 50-54) of metal (210, 230, 240, 250,) on a layer of interlayer dielectric (270) in the semiconductor device; forming a layer of TiN (205) on the final layer of metal; forming a first layer of photoresist (200) on the layer of TiN; patterning and developing the first layer of photoresist exposing portions of the layer of TiN (see figure 2A and related text); etching holes in the layer of TiN and the final

layer of metal exposing portion of interlayer dielectric (see figure 2B), wherein metal structures are formed; removing the first layer of photoresist (see figure 2B and related text); removing the remaining portions of the layer of TiN (see figure 2C); and forming a blanket layer of interlayer dielectric on the surface of the semiconductor device (280).

However, the reference does not teach depositing a second photoresist layer, patterning and etching the layer of photoresist and blanket layer to exposed the metal layer, etching the photoresist layer and TiN layer by using fluorine containing gas chemistry at an elevated temperature.

Referring to figures 1a-1I, the Admitted Prior Art teaches a method of manufacturing a semiconductor device comprises: forming a final metal layer (104) over the interlayer dielectric (102), forming a TiN layer (106) over the metal layer, forming a layer of photoresist (108) over the TiN layer, patterning and developing the first layer of photoresist exposing portions of the TiN layer, etching in the layer of TiN and the final layer of metal exposing portions of the interlay dielectric layer, removing the first layer of photoresist and the layer of TiN, depositing a blanket layer (114), forming a second photoresist layer (116) on the blanket layer of interlayer dielectric; patterning and developing the second layer of the photoresist layer exposing portions of blanket layer of interlayer dielectric overlying metal structures; and etching the exposed portion of the blanket layer of interlayer dielectric down to the metal structures, removing the second layer of the photoresist (see figures 1a-1I of the Admitted Prior art and related text).

Therefore, it would have been obvious to one of ordinary skill in the requisite art at the time the invention was made would form a second photoresist layer, patterning and etching the layer of photoresist and blanket layer to exposed the metal layer as taught by the Admitted Prior art in process of Xing et al because the technique is known in manufacturing a semiconductor device.

(11) Response to Argument

I- Appellant contends (in page 3) that none of Xing et al's layers 210, 230, 240, 250 is a final layer as defined in the present invention as the layer of metal associated with the process of manufacturing pads that provide electrical contacts to outside of the semiconductor device being manufactured. This is not found to be persuasive because applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., ***the layer of metal associated with the process of manufacturing pads that provide electrical contacts to outside of the semiconductor device being manufactured***) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant contends (in page 4) that Xing et al. leaves a layer of TiN (230), Xing et al. is not concerned with the "final layer" of metal as in the present invention. This is not found to be persuasive because layer TiN (230) is a part of the final layers 210, 230, 240, 250 and in the comprising claim it leaves the claims open for inclusion of more than one unspecified ingredients/process steps. TiN (205) is removed in figure 2C as claimed in the instant invention. See ex parte Davis et al. 80 USPQ 448.

Appellant contends (in page 4) that gold wire bonding process is not contemplated in Xing et al.. This is found not to be persuasive because applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., gold wire bonding process) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification

are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant contends (in page 4) that layer (210) is not a final metal layer. This is not found to be persuasive because layer (210) is a part of the final metal layer, wherein the final metal layer includes 210, 230, 240, and 250 (see figure 2, and the above rejection).

Appellant contends (in page 4) that the examiner is in error – the remaining portions of the TiN are not removed, the layer (unnumbered in figure 2C) over structures 240 are TiN and have not been removed. This is not found to be persuasive because layer 230 (TiN) is a part of the final layer, and layer 205 (TiN) is formed on the final layer (210, 230, 240, and 250) is completely removed (see figure 2C of Xing et al.).

Appellant contends (in page 4) that Xing et al. does not removed the layer of photoresist and the layer 205 (TiN) during the same process as does the present application. This is not found to be persuasive because applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., remove the TiN and photoresist layers ***in the same process***) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant contends (in page 4) that Xing et al. does not anticipate the present invention. This not found to be persuasive because Xing teaches:

forming a final layer (see col. 5, lines 50-54) of metal (210, 230, 240, and 250) on a layer of interlayer dielectric (270) in the semiconductor device (see figures 2A).

removing the first layer of photoresist (200) and the remaining portion of the TiN (205) in figures 2a-2c.

Appellant contends (in page 4) that Xing et al. does not teach pattern and develop the second layer of photoresist exposing portions of the blanket layer of interlayer dielectric overlying the metal structures. This is not found to be persuasive because the Admitted prior art teaches pattern and develop the second layer of photoresist (116) exposing portions of the blanket layer of interlayer dielectric overlying the metal structures (see figure 1G of the Admitted Prior Art).

Appellant contends (in page 4) that Xing et al. does not teach etching the exposed portions of the blanket layer interlayer dielectric down to the metal structure. This is not found to be persuasive because the Admitted prior art teaches etch the exposed portions of the blanket layer interlayer dielectric (see figure 1H) down to the metal structure (see figure 1I).

Appellant repeatedly contends (in page 5) that removing the TiN layer and photoresist layer are in the same process. This is not found to be persuasive because applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., remove the TiN layer and photoresist layer ***in the same process***) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

II Claims 1 and 3-4 are not patentable under 35 USC 103 over Xing et al. in view of the admitted prior art because:

Xing et al teaches a method of manufacturing a semiconductor device, wherein the method comprises: forming a final layer (see col. 5, lines 50-54) of metal (210, 230, 240, 250,) on a layer of interlayer dielectric (270) in the semiconductor device; forming a layer of TiN (205) on the final layer of metal; forming a first layer of photoresist (200) on the layer of TiN; patterning and developing the first layer of photoresist exposing portions of the layer of TiN (see figure 2A and related text); etching holes in the layer of TiN and the final layer of metal exposing portion of interlayer dielectric (see figure 2B), wherein metal structures are formed; removing the first layer of photoresist (see figure 2B and related text); removing the remaining portions of the layer of TiN (see figure 2C); and forming a blanket layer of interlayer dielectric on the surface of the semiconductor device (280).

And the Admitted Prior Art teaches a method of manufacturing a semiconductor device comprises: forming a final metal layer (104) over the interlayer dielectric (102), forming a TiN layer (106) over the metal layer, forming a layer of photoresist (108) over the TiN layer, patterning and developing the first layer of photoresist exposing portions of the TiN layer, etching in the layer of TiN and the final layer of metal exposing portions of the interlay dielectric layer, removing the first layer of photoresist and the layer of TiN, depositing a blanket layer (114), forming a second photoresist layer (116) on the blanket layer of interlayer dielectric; patterning and developing the second layer of the photoresist layer exposing portions of blanket layer of interlayer dielectric overlying metal structures; and etching the exposed portion of the blanket layer of interlayer dielectric down to the metal structures, removing the second layer of the photoresist (see figures 1a-1I of the Admitted Prior art and related text).

Appellant contends that the use of applicant's Admitted Prior Art is inappropriate. This is not found to be persuasive because applicant has a duty to disclosed any known Prior Art in his/her possession to the Office/Examiner during the prosecution.

Therefore, Examiner has clearly pointed out where critical method step limitation is present in all of cited references and therefore meets the burden under 35 USC § 103 to establish a prima facie case of obviousness.

III. Examiner refused to enter the proposed amendment after final on the ground that the new limitation 'simultaneously' contain the new subject matter. This issue relates to petitionable subject matter under 37 CFR 1.181 and not to appealable subject matter. See MPEP §§ 1002 and 1201.

For the above reasons, it is believed that the rejections should be sustained.

The conference was held on 5/8/01 in present of:

Charles Bowers (SPE) Arthur Grimley (SPE) Thanh Nguyen

Respectfully submitted,

T.N.
Thanh Nguyen
May 8, 2001

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